REMARKS

Applicant appreciates the thorough review of the present application that is evidenced in the Office Actions of December 30, 2005 and April 19, 2006. Applicant also appreciates the indication that Claims 4, 7, 12 and 24 are directed to allowable subject matter. Applicant has cancelled withdrawn Claims 13-21 and 26-28. This cancellation is done without prejudice to the filing of a divisional application for these claims. Applicant has also rewritten Claims 4, 7, 12 and 24 into independent form such that each of these claims is now in condition for allowance. Applicant has also cancelled Claims 1-2 and 22-23, amended Claims 3, 5, 8-9 and 11 to depend from Claim 4, and amended Claim 25 to depend from Claim 24. In light of these amendments, all of the remaining claims (Claims 3-12 and 24-25) are directed to subject matter that was indicated allowable in the Office Action of April 19, 2006.

I. The Objections to the Drawings

The replacement drawings filed March 17, 2006 were objected to as being non-compliant. Applicant's representative apologizes for his oversight in failing to label the drawings as "Replacement Sheets" and the failure to include "Annotated Sheets." Corrected versions of FIGS. 2 and 5 which show transistor 236 as a PMOS transistor, along with annotated versions of the corrected drawings, are enclosed herewith.

II. The Rejections Under 35 U.S.C. § 103

Claims 1-3, 5-6, 8-9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "Applicant's Admitted Prior Art" in view of Korean Patent Application No. KR2002054857A to Jung ("Jung"). (Office Action at 3-5). Claims 10, 22, 23 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art and Jung, and further in view of U.S. Patent Application Publication No. US2001/0052624 A1 to Houston ("Houston"). (Office Action at 5-6). As noted above, in light of Applicant's claim amendments, the rejections of Claims 1-2 and 22-23 have been rendered moot by the cancellation of these claims, and Claims 3, 5-6, 8-11 and 25 have been amended to depend from claims that were indicated as allowable. Thus, all of the pending claims are directed to subject matter that has been indicated as allowable.

III. Translation of Jung

Applicant has arranged to have the portion of Jung cited in the April 19, 2006 Office Action translated during Applicant's consideration of the April 19, 2006 Office Action. Applicant has not submitted this partial translation of Jung in an Information Disclosure Statement as Jung has already been considered and cited by the patent examiner as indicated on the PTO Form 892 attached to the April 19, 2006 Office Action. However, Applicant has attached to the present Amendment a copy of the partial translation of Jung so that the patent examiner may fully consider the translation during the prosecution of this case.

IV. Conclusion

As all of the pending claims are now in condition for allowance, a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,

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CERTIFICATION OF FACSIMILE TRANSMISSION UNDER 37 CFR 1.8

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Michele McMahan

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KOREAN PATENT ABSTRACT (KR)

Patent Laid-Open Gazette

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(54) Title of the Invention: Precharge Control Circuit

Technical Problem and Solution of the Related Art

Conventional precharge control circuits have the following problem.

When an abnormal glitch is generated in a precharge signal, the precharge signal is enabled before a main amplifier senses data, which causes a wrong operation of the main amplifier.

In order to resolve the problem of the convention precharge control circuits, an object of the present invention is to provide a precharge control circuit which prevents a wrong operation of a main amplifier due to timing mismatch, by controlling a precharge signal regardless of the timings of a delay signal and a precharge enable signal.

Detailed Description of the Invention

FIG. 4 is a circuit diagram of a precharge control circuit according to the present invention.

Referring to FIG. 4, the precharge control circuit includes: a first delay unit 41 for receiving a precharge control signal YIOR of a main amplifier and delaying and outputting the precharge control signal YIOR; a first inverting unit 42 for receiving the output signal of the first delay unit 41 and inverting and outputting the output signal; a second inverting unit 43 for receiving and inverting the output signal of the first inverting unit 42 and outputting the resultant signal as a precharge delay signal YIORD; a first short pulse delay unit 44 for receiving the precharge delay signal YIORD and outputting a short pulse signal having a predetermined delay time; a first NAND gate 45 for receiving and calculating the precharge delay signal YIORD and the output signal of the first short pulse delay unit 44 and outputting a set signal Mset; a third inverting unit 46 for receiving the precharge control signal YIOR of the main amplifier and inverting and outputting the precharge control signal YIOR; ã second delay unit 47 for receiving the output signal of the third inverting unit 46 and delaying and outputting the output signal; a fourth inverting unit 48 for inverting and outputting the output signal of the second delay unit 47; a second NAND gate 49 for receiving, calculating, and outputting the output signal of the third inverting unit 36 and the output signal of the fourth inverting unit 48; a fifth inverting unit 50 for receiving and inverting the output signal of the second NAND gate 49 and outputting a precharge enable signal YMAE; a sixth inverting unit

51 for receiving the precharge enable signal YMAE and inverting and outputting the precharge enable signal YMAE; a second short pulse delay unit 52 for receiving the output signal of the sixth inverting unit 51 and outputting a short pulse signal having a predetermined delay time; a third NAND gate 53 for receiving and calculating the output signal of the sixth inverting unit 51 and the output signal of the second short pulse delay unit 52 and outputting a reset signal Mreset; a latch unit 54 for receiving, calculating, and outputting the set signal Mset, the reset signal Mreset, and a reset signal RST of a memory device; and a precharge signal outputting unit 55 for receiving the output signal of the latch unit 54 and outputting a precharge signal MAPCih.

Here, in each of the first and second delay units 41 and 47, an even number of inverters are serially connected with each other. In each of the first and second short pulse delay units 44 and 52, an odd number of inverters are serially connected with each other.

Also, the latch unit 54 may be a SR latch consisting of NAND gates.

The operation of the precharge control circuit according to the present invention constructed as described above will be described below.

FIG. 5 illustrates timing diagrams of operation signals of the precharge control circuit, according to the present invention.

Referring to FIG. 5, if a reset signal RST of the memory device is enabled, a precharge delay signal YIORD delayed by predetermined delay time tD1 by a precharge control signal YIOR is generated, and the precharge delay signal YIORD generates a set signal Mset having a short pulse through the first short pulse delay unit 44 and the first NAND gate 45.

Also, a precharge enable signal YMAE delayed by a predetermined delay time tD2 by the precharge control signal YIOR is generated, and the precharge enable signal YMAE generates a reset signal Mreset having a short pulse by the second short pulse delay unit 52 and the third NAND gate 53.

A precharge signal MAPCih is set or reset by the set signal Mset and the reset signal Mreset, each having a short pulse.

Effect of the Invention

The precharge control circuit as described above has the following effect.

By controlling a precharge signal using a set signal and a reset signal, it is possible to prevent a glitch from being generated by timing mismatch between a precharge delay signal and a precharge enable signal. Accordingly, a wrong operation of a main amplifier due to the glitch can be prevented.

Annotated Sheet Showing Change(s)

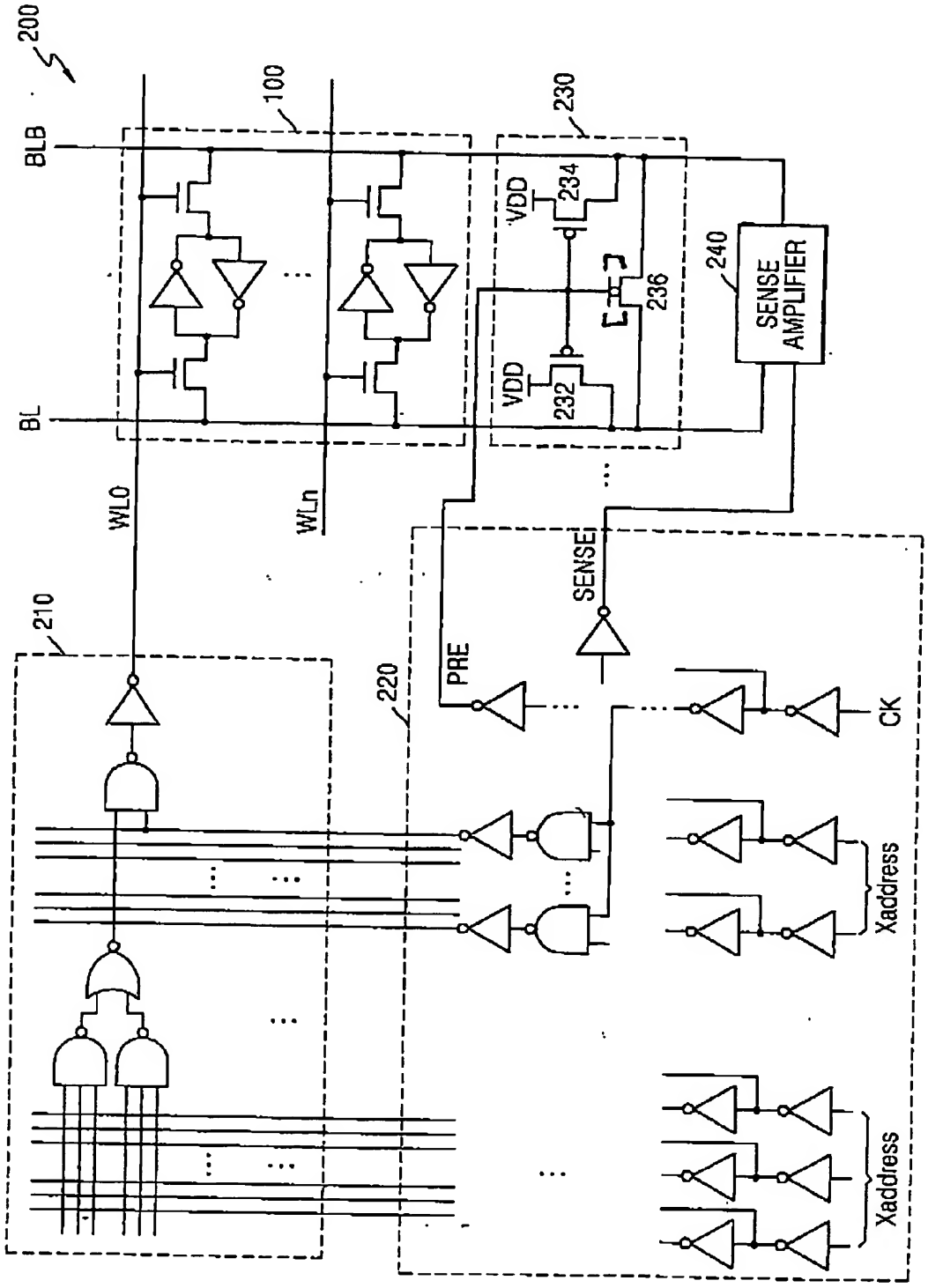

FIG. 2 (PRIOR ART)

Annotated Sheet Showing Change(s)

FIG. 5